Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1-2 (Canceled)

3. (Currently amended) A method for signal flow driven circuit physical synthesis ~~technique of claim 2,~~ the method comprising:

(a) Providing a first memory ~~that is able~~ configured to store a circuit netlist employing a set of input and output pins, ~~any other~~ a set of terminal pins, a set of power and ground terminals, a set of active device elements, and a set of passive device elements; ~~and~~

(b) Storing said circuit netlist in said first memory ~~memories~~; ~~and~~

(c) Providing a second memory ~~that is able~~ configured to store a series of technology files ~~in said memory~~; ~~and~~

(d) Storing said series of technology files in said second memory; ~~and~~

(e) Providing a third memory ~~that is able~~ configured to store a series of signal flow information generated from [[the]] a signal flow driven circuit analysis technique utilizing a software program to automatically trace signal flows of a circuit, analyze a circuit, and partition a circuit based on functionality and criticality ~~of claim 1 in said memory~~; ~~and~~

(f) Storing said series of signal flow information in said third memory; ~~and~~

(g) Providing a fourth memory ~~that is able~~ configured to store ~~said multitude~~ a set of circuit layout constraints generated from ~~a signal flow driven circuit analysis technique by tracing circuit signal flow so that, analyzing a circuit, and partitioning a circuit based on functionality and criticality, and generating a multitude set of circuit layout constraints are done by software program automatically and from~~ said signal flow information ~~in said memory~~, and to store a series of parasitic loading constraints generated from said signal flow information, and to store a series of geometry constraint generated from said signal flow information, and to store a series of proximity constraints generated from said signal flow information ~~in said memory~~; ~~and~~

(h) Storing said ~~multitude~~ set of circuit layout constraints, and said series of parasitic loading constraints, and said series of geometry constraint, and said series of proximity constraints in said fourth memory; ~~and~~

(i) Providing a fifth memory ~~that is able~~ configured to store a critical device generator ~~in said memory~~; ~~and~~

(j) Storing said critical device generator in said fifth memory; and

(k) Synthesizing a series of circuit component layouts and a series of unit circuit layouts ~~Utilizing~~ utilizing said critical device generator based on said circuit netlist, and said series of technology files, and said signal flow information, and said ~~multitude~~ set of layout constraints, and said parasitic loading constraints[[,]] ~~and said critical device generator to synthesize a series of circuit component layouts and a series of unit circuit layouts~~ while observing optimized matching, optimized area, optimized symmetry, and optimized parasitic loading requirements.

4. (Currently amended) The method of claim 3 ~~signal flow driven circuit physical synthesis technique of claim 2~~ further ~~including a signal flow driven circuit cell placement methodology~~ comprising:

(a) Providing a sixth memory ~~that is able~~ configured to store a placement module~~;~~ ~~in said memory~~[[.]]

(b) Storing said placement module in said sixth memory; ~~and~~

(c) Providing a seventh memory ~~that is able~~ configured to store a series of matching requirements of a series of devices associated with a critical signal flow path and a series of symmetry requirements of said series of devices associated with said critical signal flow path in said memory; ~~and~~

(d) Generating a layout of said circuit ~~Utilizing~~ utilizing said placement module ~~and the signal flow driven circuit physical synthesis technique of claim 3 wherein~~ based on said series of circuit component layouts and ~~wherein~~ said series of unit circuit layouts to ~~layout said circuit providing~~ provide minimized separations of the circuit component layouts and the unit circuit layouts in said critical signal flow path; and

(e) Placing a series of non-critical components in said layout ~~Utilizing~~ utilizing said placement module ~~to place a series of non-critical components in rest of said area;~~

~~Whereby an engineer can achieve compact layout for an analog circuit, a mixed signal circuit, and a RF circuit automatically~~.

5. (Currently amended) The method of claim 3 ~~signal flow driven circuit physical synthesis technique of claim 2~~ further ~~including a signal flow driven circuit cell routing methodology~~ comprising:

(a) Proving a sixth memory ~~that is able~~ configured to store a routing module ~~in said memory;~~ ~~and~~

(b) Storing said routing module in said sixth memory; ~~and~~

(c) Providing a seventh memory ~~that is able~~ configured to store a series of parasitic loading constraints of ~~multitude~~ a set of circuit nodes of a critical signal flow path ~~in said memory~~; and

(d) Connecting a series of critical nets in said critical signal flow path of said circuit before connecting a series of non-critical nets in said circuit ~~Utilizing~~ utilizing said routing module[[,]] ~~and~~ based on said series of parasitic loading constraints, and ~~the signal flow driven circuit physical synthesis technique of claim 3 wherein~~ said series of geometry constraints, and said series of proximity constraints ~~to connect a series of critical nets in said critical signal flow path of said circuit before connecting a series of non-critical nets in said circuit;~~

~~Whereby an engineer can route an analog circuit, a mixed signal circuit, and a RF circuit automatically~~.

6. (Currently amended) A ~~mean of~~ system for circuit performance assurance, the system comprising ~~utilizing~~:

~~(a) a signal flow driven circuit analysis technique by tracing circuit signal flow so that, analyzing a circuit, and partitioning a circuit based on functionality and criticality, and generating multitude circuit layout constraints are done by software program automatically, and~~

~~(b) The signal flow driven circuit physical synthesis technique of claim 2, and~~

~~(c) The signal flow driven circuit cell placement methodology of claim 4, and~~

~~(d) The signal flow driven circuit cell routing methodology of claim 5~~

means for generating a set of circuit layout constraints using a signal flow driven circuit analysis in response to automatically analyzing a circuit and partitioning the circuit based on functionality and criticality;

means for synthesizing a series of circuit component layouts and a series of unit circuit layouts using a signal flow driven physical synthesis technique based on a circuit netlist, a series of technology files, signal flow information, a set of layout constraints, and parasitic loading constraints while observing optimized matching, optimized area, optimized symmetry, and optimized parasitic loading requirements;

means for generating a layout for the circuit using a signal flow driven circuit cell placement technique in response to the series of circuit component layouts and the series of unit circuit layouts to provide minimized separations of the circuit component layouts and the unit circuit layouts in the critical signal flow path;

means for placing a series of non-critical components in the layout; and

means for connecting a series of critical nets in the critical signal flow path of the circuit using a signal flow driven circuit cell routing technique before connecting a series of non-critical nets in the circuit based on the series of parasitic loading constraints, a series of geometry constraints, and a series of proximity constraints.

7. (Currently amended) A ~~mean~~ method for circuit physical layout floor planning ~~utilizing~~, the method comprising:

~~(a) a signal flow driven circuit analysis technique by tracing circuit signal flow so that, analyzing a circuit, and partitioning a circuit based on functionality and criticality, and generating multitude circuit layout constraints are done by software program automatically;~~

~~(b) The signal flow driven circuit physical synthesis technique of claim 2, and~~

~~(c) The signal flow driven circuit cell placement methodology of claim 4, and~~

~~(d) The signal flow driven circuit cell routing methodology of claim 5~~

generating a set of circuit layout constraints using a signal flow driven circuit analysis in response to automatically analyzing a circuit and partitioning the circuit based on functionality and criticality;

synthesizing a series of circuit component layouts and a series of unit circuit layouts using a signal flow driven physical synthesis technique based on a circuit netlist, a series of technology files, signal flow information, a set of layout constraints, and parasitic loading constraints while observing optimized matching, optimized area, optimized symmetry, and optimized parasitic loading requirements;

generating a layout for the circuit using a signal flow driven circuit cell placement technique in response to the series of circuit component layouts and the series of unit circuit layouts to provide minimized separations of the circuit component layouts and the unit circuit layouts in the critical signal flow path;

placing a series of non-critical components in the layout; and

connecting a series of critical nets in the critical signal flow path of the circuit using a signal flow driven circuit cell routing technique before connecting a series of non-critical nets in the circuit based on the series of parasitic loading constraints, a series of geometry constraints, and a series of proximity constraints.

8. (Currently amended) ~~A mean of incorporating an in-situ parasitic extraction process having the signal flow driven circuit cell routing methodology~~ The method of claim 5 further comprising ~~wherein~~ utilizing said routing module ~~incorporated~~ in [[said]] an in-situ parasitic extraction process to connect said series of critical nets in said critical signal flow path of said circuit before connecting said series of non-critical nets in said circuit.

9. (New) The method of claim 4 wherein generating said layout of said utilizing said placement module comprises automatically generating an area optimized layout of an analog circuit.

10. (New) The method of claim 4 wherein generating said layout of said utilizing said placement module comprises automatically generating an area optimized layout of a mixed signal circuit.

11. (New) The method of claim 4 wherein generating said layout of said utilizing said placement module comprises automatically generating an area optimized layout of an RF circuit.

12. (New) The method of claim 5 wherein connecting said series of critical nets in said critical signal flow path of said circuit utilizing said routing module comprises automatically routing an analog circuit.

13. (New) The method of claim 5 wherein connecting said series of critical nets in said critical signal flow path of said circuit utilizing said routing module comprises automatically routing a mixed signal circuit.

14. (New) The method of claim 5 wherein connecting said series of critical nets in said critical signal flow path of said circuit utilizing said routing module comprises automatically routing an RF circuit.

15. (New) A tangible computer-readable medium configured to store a software program having a set of modules executable by a processor of a computer system, the computer-readable medium comprising:

code for generating a set of circuit layout constraints using a signal flow driven circuit analysis in response to automatically analyzing a circuit and partitioning the circuit based on functionality and criticality; and

code for synthesizing a series of circuit component layouts and a series of unit circuit layouts using a signal flow driven physical synthesis technique based on a circuit netlist, a series of technology files, signal flow information, a set of layout constraints, and parasitic

loading constraints while observing optimized matching, optimized area, optimized symmetry, and optimized parasitic loading requirements.

16. (New) The computer-readable medium of claim 15 further comprising:

code for generating a layout for the circuit using a signal flow driven circuit cell placement technique in response to the series of circuit component layouts and the series of unit circuit layouts to provide minimized separations of the circuit component layouts and the unit circuit layouts in the critical signal flow path; and

code for placing a series of non-critical components in the layout.

17. (New) The computer-readable medium of claim 15 further comprising:

code for connecting a series of critical nets in the critical signal flow path of the circuit using a signal flow driven circuit cell routing technique before connecting a series of non-critical nets in the circuit based on the series of parasitic loading constraints, a series of geometry constraints, and a series of proximity constraints.

18. (New) The computer-readable medium of claim 15 wherein the circuit comprises a mixed signal circuit.

19. (New) The computer-readable medium of claim 15 wherein the circuit comprises an RF circuit.

20. (New) The computer-readable medium of claim 15 wherein the circuit comprises analog circuit.